AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1.-8. (Cancelled)

9. (Currently amended) A method of forming non-volatile semiconductor memory device, comprising:

providing a semiconductor substrate having a core region comprising memory cells and a peripheral region, wherein word lines in the core region connecting the memory cells are spaced apart by about 1 μm or less;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place and without masking the other transistors, heavily doping source and drain regions for the electrostatic discharge protection transistors to provide channel lengths for the electrostatic protection transistors of about 1 μm or less.

10. (Cancelled)

11. (Previously presented) The method of claim 9, wherein heavily doping source and drain regions involves implanting with one of arsenic and phosphorus at about 5 x 10^{14} atoms/cm^2 to about 7 x 10^{15} atoms/cm^2 at an energy from about 60 keV to about 100 keV.

12. (Previously presented) The method of claim 9, wherein the non-volatile semiconductor memory device is a SONOS type flash memory device.

13. (Original) The method of claim 12, wherein the flash memory device comprises a virtual ground array structure and SONOS type memory cells.

14. (Cancelled)

15. (Cancelled)

16. (Previously presented) The method of claim 9, wherein heavily doping source and drain regions involves implanting with one of arsenic and phosphorus at about 1 x 10^{14} atoms/cm^2 to about 1 x 10^{16} atoms/cm^2 at an energy from about 60 keV to about 100 keV.

17. (Currently amended) A method of forming non-volatile semiconductor memory device, comprising:

providing a semiconductor substrate having a core region comprising memory cells and a peripheral region, wherein word lines in the core region connecting the memory cells are spaced apart by about 1 μm or less;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

lightly doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic, boron, and phosphorus at about 1×10^{11} atoms/cm^2 to about 1×10^{14} atoms/cm^2 at an energy from about 20 keV to about 80 keV;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place and without masking the other transistors, heavily doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic and phosphorus at about 1×10^{14} atoms/cm^2 to about 1×10^{16} atoms/cm^2 at an energy from about 60 keV to about 100 keV to provide channel lengths for the electrostatic protection transistors of about 0.25 μm or less.

18. (Currently amended) A method of forming non-volatile semiconductor memory device, comprising:

providing a semiconductor substrate having a core region comprising memory cells and a peripheral region, wherein word lines in the core region connecting the memory cells are spaced apart by about 1 μm or less;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

lightly doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic, boron, and phosphorus at about 1×10^{11} atoms/cm^2 to about 1×10^{14} atoms/cm^2 at an energy from about 20 keV to about 80 keV;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place and without masking the other transistors, heavily doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic and phosphorus at about 5×10^{14} atoms/cm^2 to about 7×10^{15} atoms/cm^2 at an energy from about 60 keV to about 100 keV to provide channel lengths for the electrostatic protection transistors of about 0.25 μm or less.

19. (New) The method of claim 9, wherein the channel lengths of the electrostatic protection transistors are about 0.25 μm or less.

20. (New) The method of claim 9, wherein the channel lengths of the electrostatic protection transistors are about 0.15 μm or less.

21. (New) The method of claim 9, wherein the word lines in the core region connecting the memory cells are spaced apart by about 0.2 μm to about 0.75 μm.

22. (New) The method of claim 11, wherein heavily doping source and drain regions for the electrostatic discharge protection transistors comprises doping with arsenic.

23. (New) The method of claim 11, wherein heavily doping source and drain regions for the electrostatic discharge protection transistors comprises doping with phosphorus.

24. (New) The method of claim 17, wherein the non-volatile semiconductor memory device is a SONOS type flash memory device.

25. (New) The method of claim 17, wherein heavily doping source and drain regions for the electrostatic discharge protection transistors comprises doping with arsenic.

26. (New) The method of claim 17, wherein the channel lengths of the electrostatic protection transistors are about 0.15 μm or less.

27. (New) The method of claim 17, wherein the word lines in the core region connecting the memory cells are spaced apart by about 0.2 μm to about 0.75 μm.

28. (New) The method of claim 18, wherein the non-volatile semiconductor memory device is a SONOS type flash memory device.

29. (New) The method of claim 18, wherein the channel lengths of the electrostatic protection transistors are about 0.15 μm or less.

30. (New) The method of claim 18, wherein the word lines in the core region connecting the memory cells are spaced apart by about 0.2 μm to about 0.75 μm.

31. (New) The method of claim 18, wherein heavily doping source and drain regions for the electrostatic discharge protection transistors comprises doping with phosphorus.